

**IN THE CLAIMS**

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

- 1 1. (Currently Amended) A wireless transceiver device, comprising:  
2 modulation circuitry for modulating and demodulating signals that are transmitted over ~~the~~  
3 ~~airwaves~~ airwaves;  
4 frequency conversion circuitry for up converting and down converting between radio frequency  
5 signals and baseband frequency signals;  
6 digital-to-analog conversion circuitry for converting from analog to digital and from digital to  
7 analog;  
8 a radio controller; ~~and~~  
9 baseband processing circuitry including a first in, first out (FIFO) memory structure for storing  
10 addresses for accessing data blocks; and  
11 a plurality of command blocks formed within a memory structure, the command blocks include  
12 addresses of data blocks stored within random access memory and a memory portion for storing an  
13 indicator for indicating whether a command block of the plurality of command blocks is in use.

Claim 2. (Cancelled)

- 1 3. (Currently Amended) The ~~wireless transceiver~~ wireless transceiver device of claim 1  
2 wherein the ~~first in, first out~~ FIFO memory structure includes pointers that define addresses of the  
3 command blocks.

Claim 4. (Cancelled)

- 1 5. (Currently Amended) The ~~wireless transceiver~~ wireless transceiver device of claim 1 wherein the  
2 modulation circuitry includes Gaussian Phase Shift Keying modulation and demodulation circuitry.
- 1 6. (Currently Amended) The ~~wireless transceiver~~ wireless transceiver device of claim 1 wherein the  
2 frequency conversion circuitry converts directly between radio frequency and baseband.

1 7. (Currently Amended) A method for storing and transmitting data, comprising:  
2 storing a data block in random access memory; and  
3 storing a pointer that corresponds to the data block in a first in, first out (FIFO) memory structure,  
4 the pointer includes an address of a command block;  
5 storing an address of the data block in the command block; and  
6 setting an indicator signal in a defined memory location, wherein the indicator signal indicates  
7 that the data block address stored in the command block is for data that has yet to be successfully  
8 transmitted and that the command block is busy.

Claims 8-10. (Cancelled)

1 11. (Currently Amended) The method of ~~claim 10~~ claim 7 wherein an address for a data block is only  
2 stored in a command block if ~~an indicator~~ the indicator signal reflects that the command block does not  
3 contain the address of a data block that has yet to be successfully transmitted.

1 12. (Currently Amended) The method of claim 7 further ~~including the step of~~ comprises:  
2 ~~evaluating a command block address stored within a~~ the command block address included within  
3 the FIFO pointer.

1 13. (Currently Amended) The method of claim 12 further ~~including~~ comprises:  
2 examining the contents of the command block specified by the pointer to determine a data block  
3 address.

1 14. (Currently Amended) The method of claim 13 further ~~including the step of~~ comprises:  
2 evaluating at least ~~the first memory location~~ a first memory location of the data block whose  
3 address ~~is specified in~~ is stored in the command block to determine ~~the size of the data block~~ a data block  
4 size.

1 15. (Currently Amended) The method of claim 14 further ~~including the step of~~ comprises:  
2 retrieving an amount of data corresponding to the ~~size data block specified in claim 14~~ data block  
3 size and transmitting that data to a radio modem for transmission over ~~a wireless airwaves~~ wireless  
4 airwaves.

1 16. (Currently Amended) The method of claim 15 further ~~including the step of~~ comprises:  
2 resetting the indicator signal if the transmission was successful.

1 17. (Currently Amended) A memory structure formed within a baseband processing system,  
2 comprising:  
3 a random access memory portion for storing data blocks that are to be transmitted in a first in,  
4 first out (FIFO) order; and a ~~first in, first out~~ FIFO memory structure for storing pointers that correspond  
5 to the data blocks stored in the random access memory portion;  
6 a plurality of command blocks defined within the random access memory portion wherein each  
7 command block is for specifying an address of a data block that is to be transmitted; and  
8 a defined memory portion for storing command block indicators for each command block,  
9 wherein the command block indicators specify whether its corresponding command block includes the  
10 address of a data block that has yet to be transmitted successfully.

Claims 18-19. (Cancelled)

1 20. (Currently Amended) The memory structure of ~~claim 19~~ claim 17 wherein the ~~memory portions~~  
2 defined memory portions for storing the ~~indicators~~ command block indicators are each one bit in length.

1 21. (Currently Amended) The memory structure of ~~claim 18~~ claim 17 wherein the command blocks  
2 defined within the random access memory portions ~~for storing the command blocks~~ are each four bytes in  
3 length.

1 22. (Currently Amended) The memory structure of claim 17 wherein the ~~first in, first out~~ FIFO  
2 memory structure defines a plurality of ~~first in, first out~~ FIFO memory blocks wherein each ~~first in, first~~  
3 ~~out memory~~ FIFO memory block relates to data blocks that are to be transmitted to a particular device.